Listing of the Claims

This Listing of the Claims will replace all prior versions and listings of claims in this application.

Claims 1 – 3 (Cancelled)

4. (New) A method of forming a graded junction in a semiconductor substrate utilizing an integrated circuit fabrication technique that is characterized by a minimum geometry feature, the semiconductor substrate having a first conductivity type, the method comprising:

introducing a dopant into a first region of the semiconductor substrate to form a primary dopant region, the primary dopant region having a second conductivity type that is opposite the first conductivity type, the primary dopant region having a first dopant concentration, the perimeter of the primary dopant region defining a primary junction between the primary dopant region and the semiconductor substrate;

simultaneously with forming the primary dopant region, introducing the dopant into a second region of the semiconductor substrate to form a perimeter dopant region having the second conductivity type in the semiconductor substrate around the perimeter of the primary dopant region and spaced-apart from the primary junction by a distance that is less than two times (2x) the lateral diffusion length of the primary junction during a thermal diffusion step that is part of the integrated circuit fabrication technique, the perimeter dopant region having a second dopant concentration that is less than the first dopant concentration; and

performing the thermal diffusion step such that the dopant in the primary dopant region and the dopant in the perimeter dopant region diffuse to merge to provide a graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration.

5. (New) A method of forming a graded junction in a semiconductor substrate utilizing an integrated circuit fabrication technique that is characterized by a minimum geometry feature, the semiconductor substrate having a first conductivity type, the method comprising:

forming a patterned mask on an upper surface of the semiconductor substrate, the mask including a first opening that exposes a first upper surface area of the semiconductor substrate and a second opening that defines a perimeter upper surface area that surrounds and is spaced-apart from the first upper surface area by a distance that is less than two times (2x) the lateral diffusion length of the dopant in the semiconductor substrate during a thermal diffusion step that is part of the integrated circuit fabrication technique, the second opening having the minimum geometry feature;

in a single ion implant step, utilizing the mask to implant dopant having a second conductivity type opposite the first conductivity type into the first upper surface area of the semiconductor material to define a primary dopant region therein and into the perimeter upper surface area of the semiconductor material to define a perimeter dopant ring therein that is spaced-apart from the primary dopant region thereby defining a primary junction between the primary dopant region and the semiconductor material; and

performing the thermal diffusion step such that the dopant in the primary dopant region and in the perimeter dopant ring diffuse to merge to provide a graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration.

6. (New) A method of forming a graded junction in a semiconductor substrate utilizing an integrated circuit fabrication technique that is characterized by a minimum geometry eture, the semiconductor substrate having a first conductivity type, the method comprising:

forming a patterned mask on an upper surface of the semiconductor substrate, the mask including a first opening that exposes a first upper surface area of the semiconductor substrate and a second set of openings that define a plurality of quadrilateral island areas on the upper surface of the semiconductor substrate, the island areas being disposed around and spaced-apart from the perimeter of the first upper surface area by a distance that is less than two times (2x) the

lateral diffusion length of a dopant in the semiconductor substrate during a thermal diffusion step that is part of the integrated circuit fabrication technique, each of the plurality of island areas having the minimum geometry feature;

in a single ion implant step, utilizing the mask to implant the dopant into the first upper surface area of the semiconductor substrate to define a primary dopant region therein and into the upper surface island areas of the semiconductor substrate to define a plurality of quadrilateral perimeter dopant islands therein that are spaced-apart from the primary dopant region, thereby defining a primary junction between the primary dopant region and the semiconductor material; and

performing the thermal diffusion step such that the dopant in the primary dopant region and in the perimeter dopant islands diffuses to merge to provide a graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration.